Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SIGNAL PAD X/Y COORDINATES PAD SIZE**

**NAME NUMBER X Y X Y**

**INPUT - 1 -791 493 80 x 80**

**INPUT + 2 -791 -490 80 x 80**

**NC 3 -296 -530 55 x 55**

**NC 4 -172 -530 55 x 55**

**NC 5 -47 -530 55 x 55**

**NC 6 79 -530 55 x 55**

**NC 7 207 -529 55 x 55**

**V - 8 358 -520 80 x 80**

**V - 9 777 -528 220 x 80**

**OUTPUT 10 791 0 80 x 220**

**V + 11 777 458 220 x 220**

**V + 12 358 520 80 x 80**

**NC 13 207 529 55 x 55**

**NC 14 79 530 55 x 55**

**NC 15 -47 530 55 x 55**

**NC 16 -172 530 55 x 55**

**NC 17 -296 530 55 x 55**

**17 16 15 14 13 12**

**3 4 5 6 7 8**

**1**

**2**

**11**

**10**

**9**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: None**

**APPROVED BY: DK DIE SIZE .051” X .076” DATE: 12/11/17**

**MFG: NATIONAL THICKNESS .016” P/N: LM7171**

**DG 10.1.2**

#### Rev B, 7/1